Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (CANCELLED).

2. (CURRENTLY AMENDED) ~~The method of claim 1, wherein~~ A method for selectively masking off undesirable states in selected scan cells, which cause test failures, from being compacted in selected pattern compactors for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, an output-mask controller, and an output-mask network, each scan chain comprising multiple scan cells coupled in series, the output-mask controller including a combinational output controller connected to the output-mask network, the combinational output controller comprising one or more selected combinational logic networks other than a complete network of AND gates; said method comprising:

(a) generating and shifting in a stimulus through said pattern generators to all said scan cells in said scan-based integrated circuit during a shift-in operation; said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises generating a compressed stimulus, decompressing said compressed stimulus as said stimulus through said pattern generators, and shifting in said stimulus to all said scan cells in said selected scan-test mode during said shift-in operation; wherein said compressed stimulus is selectively generated internally or supplied externally from an ATE (automatic test equipment)[[.]];

(b) capturing a test response to all said scan cells during a selected capture operation;

(c) shifting out said test response or said stimulus to said pattern compactors for compaction by selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors using said output-mask controller and said output-mask network, while shifting in a new stimulus to all said scan cells, during a shift-out operation; and

(d) repeating steps (b) to (c) until a predetermined limiting criteria is reached.

3. (ORIGINAL) The method of claim 2, wherein each said pattern generator is selectively a broadcaster or a decompressor.

Claims 4 and 5 (CANCELLED).

6. (CURRENTLY AMENDED) ~~The method of claim 1, wherein~~ A method for selectively masking off undesirable states in selected scan cells, which cause test failures, from being compacted in selected pattern compactors for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, an output-mask controller, and an output-mask network, each scan chain comprising multiple scan cells coupled in series, the output-mask controller including a combinational output controller connected to the output-mask network, the combinational output controller comprising one or more selected combinational logic networks other than a complete network of AND gates; said method comprising:

(a) generating and shifting in a stimulus through said pattern generators to all said scan cells in said scan-based integrated circuit during a shift-in operation; said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises using a load signal to preset said output-mask controller with a predetermined state for selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors during a selected shift-in operation[[.]];

(b) capturing a test response to all said scan cells during a selected capture operation;

(c) shifting out said test response or said stimulus to said pattern compactors for compaction by selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors using said output-mask controller and said output-mask network, while shifting in a new stimulus to all said scan cells, during a shift-out operation; and

(d) repeating steps (b) to (c) until a predetermined limiting criteria is reached.

Claims 7 and 8 (CANCELLED).

9. (CURRENTLY AMENDED) ~~The method of claim 7, wherein~~ A method for selectively masking off undesirable states in selected scan cells, which cause test failures, from being compacted in selected pattern compactors for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, an output-mask

controller, and an output-mask network, each scan chain comprising multiple scan cells coupled in series, the output-mask controller including a combinational output controller connected to the output-mask network, the combinational output controller comprising one or more selected combinational logic networks other than a complete network of AND gates; said method comprising:

(a) generating and shifting in a stimulus through said pattern generators to all said scan cells in said scan-based integrated circuit during a shift-in operation; said shifting out said test response or said stimulus to said pattern compactors for compaction further comprises using said output-mask controller to generate a plurality of output-mask enable signals for controlling said output-mask network for selectively mask off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors during said shift-out operation; said output-mask controller further comprises a sequential output controller for generating a plurality of sequential-mask signals and said combinational output controller for generating said output-mask enable signals[[.]];

(b) capturing a test response to all said scan cells during a selected capture operation;

(c) shifting out said test response or said stimulus to said pattern compactors for compaction by selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors using said output-mask controller and said output-mask network, while shifting in a new stimulus to all said scan cells, during a shift-out operation; and

(d) repeating steps (b) to (c) until a predetermined limiting criteria is reached.

10. (ORIGINAL) The method of claim 9, wherein said sequential output controller in said output-mask controller further comprises a plurality of selected cell-mask controllers for generating one or more selected cell-mask signals, a plurality of selected chain-mask controllers for generating one or more selected chain-mask signals, and a plurality of selected pattern-mask controllers for generating one or more selected pattern-mask signals; wherein said selected cell-mask signals, said selected chain-mask signals, and said selected pattern-mask signals are collectively referred to as said sequential-mask signals.

11. (ORIGINAL) The method of claim 10, wherein each said cell-mask controller in said sequential output controller is a first finite-state machine generating one or more said selected cell-mask signals.

12. (ORIGINAL) The method of claim 11, wherein said first finite-state machine is selectively a ring counter (RC) or a first range comparator.

13. (ORIGINAL) The method of claim 10, wherein each said chain-mask controller in said sequential output controller is a second finite-state machine generating one or more said selected chain-mask signals.

14. (ORIGINAL) The method of claim 13, wherein said second finite-state machine is selectively a first shift register (SR) or a range decoder.

15. (ORIGINAL) The method of claim 10, wherein each said pattern-mask controller in said sequential output controller is a

third finite-state machine generating one or more said selected pattern-mask signals.

16. (ORIGINAL) The method of claim 15, wherein said third finite-state machine is selectively a second shift register (SR) or a second range comparator.

17. (ORIGINAL) The method of claim 9, wherein said combinational output controller, comprising one or more said selected combinational logic networks other than said complete network of AND gates, further accepts said sequential-mask signals as inputs for generating said output-mask enable signals for controlling said output-mask network for selectively masking off all said undesirable states in said selected scan cells from being compacted in said selected pattern compactors during said shift-out operation.

18. (ORIGINAL) The method of claim 17, wherein each said selected combinational logic network further comprises one or more first selected combinational gates; wherein each said first selected combinational gate is selectively an AND gate, OR gate, NAND gate, NOR gate, Exclusive-OR (XOR) gate, Exclusive-NOR (XNOR) gate, multiplexor (MUX), or inverter (INV).

Claim 19 (CANCELLED).

20. (CURRENTLY AMENDED) ~~The method of claim 1, wherein~~ A method for selectively masking off undesirable states in selected scan cells, which cause test failures, from being compacted in selected pattern compactors for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit

containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, an output-mask controller, and an output-mask network, each scan chain comprising multiple scan cells coupled in series, the output-mask controller including a combinational output controller connected to the output-mask network, the combinational output controller comprising one or more selected combinational logic networks other than a complete network of AND gates; said method comprising:

(a) generating and shifting in a stimulus through said pattern generators to all said scan cells in said scan-based integrated circuit during a shift-in operation; each said pattern compactor is selectively a multi-input signature register (MISR) or a linear compactor; wherein said linear compactor further includes one or more third selected combinational gates; wherein each said third selected combinational gate is selectively an Exclusive-OR (XOR) gate or Exclusive-NOR (XNOR) gate[[.]];

(b) capturing a test response to all said scan cells during a selected capture operation;

(c) shifting out said test response or said stimulus to said pattern compactors for compaction by selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors using said output-mask controller and said output-mask network, while shifting in a new stimulus to all said scan cells, during a shift-out operation; and

(d) repeating steps (b) to (c) until a predetermined limiting criteria is reached.

Claims 21 - 23 (CANCELLED).

24. (CURRENTLY AMENDED) ~~The output-mask controller of claim 21,~~ An output-mask controller for generating a plurality of output-mask enable signals for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, and an output-mask network, each scan chain comprising multiple scan cells coupled in series; said output-mask controller comprising:

(a) a sequential output controller for generating a plurality of sequential-mask signals; wherein said sequential output controller further comprises a plurality of selected cell-mask controllers for generating one or more selected cell-mask signals, a plurality of selected chain-mask controllers for generating one or more selected chain-mask signals, and a plurality of selected pattern-mask controllers for generating one or more selected pattern-mask signals; wherein said selected cell-mask signals, said selected chain-mask signals, and said selected pattern-mask signals are collectively referred to as said sequential-mask signals[[.]]; and

(b) a combinational output controller, comprising one or more selected combinational logic networks other than a complete network of AND gates, for generating a plurality of output-mask enable signals for controlling said output-mask network for selectively masking off undesirable states in selected scan cells, which cause test failure, from being compacted in selected pattern compactors.

25. (ORIGINAL) The output-mask controller of claim 24, wherein each said cell-mask controller in said sequential output controller is a first finite-state machine generating one or more said selected cell-mask signals.

26. (ORIGINAL) The output-mask controller of claim 25, wherein said first finite-state machine is selectively a ring counter (RC) or a first range comparator.

27. (ORIGINAL) The output-mask controller of claim 24, wherein each said chain-mask controller in said sequential output controller is a second finite-state machine generating one or more selected chain-mask signals.

28. (ORIGINAL) The output-mask controller of claim 27, wherein said second finite-state machine is selectively a first shift register (SR) or a range decoder.

29. (ORIGINAL) The output-mask controller of claim 24, wherein each said pattern-mask controller in said sequential output controller is a third finite-state machine generating one or more said selected pattern-mask signals.

30. (ORIGINAL) The output-mask controller of claim 29, wherein said third finite-state machine is second shift register (SR) or a second range comparator.

31. (CURRENTLY AMENDED) ~~The output-mask controller of claim 21,~~ An output-mask controller for generating a plurality of output-mask enable signals for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, and an output-mask network, each scan chain comprising multiple scan cells coupled in series; said output-mask controller comprising:

(a) a sequential output controller for generating a plurality of sequential-mask signals; wherein said combinational output controller, comprising one or more said selected combinational logic networks other than said complete network of AND gates, further accepts said sequential-mask signals as inputs for generating said output-mask enable signals for controlling said output-mask network for selectively masking off said undesirable states in said selected scan cells from being compacted in said selected pattern compactors[[.]]; and

(b) a combinational output controller, comprising one or more selected combinational logic networks other than a complete network of AND gates, for generating a plurality of output-mask enable signals for controlling said output-mask network for selectively masking off undesirable states in selected scan cells, which cause test failure, from being compacted in selected pattern compactors.

32. (ORIGINAL) The output-mask controller of claim 31, wherein each said selected combinational logic network further comprises one or more first selected combinational gates; wherein each said first selected combinational gate is selectively an AND gate, OR gate, NAND gate, NOR gate, Exclusive-OR (XOR) gate, Exclusive-NOR (XNOR) gate, multiplexor (MUX), or inverter (INV).

Claim 33 (CANCELLED).

Claim 34 - 49 (CANCELLED).

Claim 50 (CANCELLED).

51. ~~The method of claim 50, wherein~~ A method for selectively driving selected constant logic values into all scan cells in

selected scan chains for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, an input chain-mask controller, and an input-mask network, each scan chain comprising multiple scan cells coupled in series, the input chain-mask controller connected to the input-mask network; said method comprising:

(a) generating and shifting in a stimulus through said pattern generators to all said scan cells in said scan-based integrated circuit by selectively forcing said selected constant logic values into all said scan cells in said selected scan chains during a shift-in operation; said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises generating a compressed stimulus, decompressing said compressed stimulus as said stimulus through said pattern generators, and shifting in said stimulus to all said scan cells in said selected scan-test mode during said shift-in operation; wherein said compressed stimulus is selectively generated internally or supplied externally from an ATE (automatic test equipment)[[.]];

(b) capturing a test response to all said scan cells during a selected capture operation;

(c) shifting out said test response or said stimulus to said pattern compactors for compaction, while shifting in a new stimulus to all said scan cells in said scan-based integrated circuit, during a shift-out operation; and

(d) repeating steps (b) to (c) until a predetermined limiting criteria is reached.

52. (ORIGINAL) The method of claim 51, wherein each said pattern generator is selectively a broadcaster or a decompressor.

Claim 53 (CANCELLED).

54. (CURRENTLY AMENDED) ~~The method of claim 53,~~ A method for selectively driving selected constant logic values into all scan cells in selected scan chains for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, an input chain-mask controller, and an input-mask network, each scan chain comprising multiple scan cells coupled in series, the input chain-mask controller connected to the input-mask network; said method comprising:

(a) generating and shifting in a stimulus through said pattern generators to all said scan cells in said scan-based integrated circuit by selectively forcing said selected constant logic values into all said scan cells in said selected scan chains during a shift-in operation; wherein said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises automatically generating said stimulus internally using said pattern generators in said selected self-test mode during said shift-in operation; wherein each said pattern generator is selectively a pseudorandom pattern generator (PRPG) or a random pattern generator (RPG)[[.]];

(b) capturing a test response to all said scan cells during a selected capture operation;

(c) shifting out said test response or said stimulus to said pattern compactors for compaction, while shifting in a new stimulus to all said scan cells in said scan-based integrated circuit, during a shift-out operation; and

(d) repeating steps (b) to (c) until a predetermined limiting criteria is reached.

55. (ORIGINAL) The method of claim 50, wherein said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises using a load signal to preset said input chain-mask controller with a predetermined state to selectively force said selected constant logic values into all said scan cells in said selected scan chains during a selected shift-in operation.

56. (ORIGINAL) The method of claim 50, wherein said generating and shifting in a stimulus through said pattern generators to all said scan cells further comprises using said input chain-mask controller to generate a plurality of input-mask enable signals for controlling said input-mask network to selectively force said selected constant logic values into all said scan cells in said selected scan chains during said shift-in operation.

57. (ORIGINAL) The method of claim 56, wherein said input chain-mask controller further comprises using an initialize signal to prevent said input-mask enable signals from forcing said selected constant logic values into all said scan cells in said selected scan chains.

58. (ORIGINAL) The method of claim 56, wherein said input chain-mask controller is a finite-state machine generating said input-mask enable signals.

59. (ORIGINAL) The method of claim 58, wherein said finite-state machine is selectively a shift register (SR) or a range decoder.

Claim 60 (CANCELLED).

61. ~~The method of claim 50, wherein~~ A method for selectively driving selected constant logic values into all scan cells in selected scan chains for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, an input chain-mask controller, and an input-mask network, each scan chain comprising multiple scan cells coupled in series, the input chain-mask controller connected to the input-mask network; said method comprising:

(a) generating and shifting in a stimulus through said pattern generators to all said scan cells in said scan-based integrated circuit by selectively forcing said selected constant logic values into all said scan cells in said selected scan chains during a shift-in operation; wherein each said pattern compactor is selectively a multi-input signature register (MISR) or a linear compactor; wherein said linear compactor further includes one or more second selected combinational gates; wherein each said second selected combinational gate is selectively an Exclusive-OR (XOR) gate or Exclusive-NOR (XNOR) gate[[.]];

(b) capturing a test response to all said scan cells during a selected capture operation;

(c) shifting out said test response or said stimulus to said pattern compactors for compaction, while shifting in a new

stimulus to all said scan cells in said scan-based integrated circuit, during a shift-out operation; and

(d) repeating steps (b) to (c) until a predetermined limiting criteria is reached.

Claim 62 (CANCELLED).

63. (CURRENTLY AMENDED) ~~The input chain-mask controller of claim 62,~~ An input chain-mask controller for generating a plurality of input-mask enable signals for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, and an input-mask network, each scan chain comprising multiple scan cells coupled in series; said input chain-mask controller comprising:

a finite-state machine for generating said input-mask enable signals for controlling said input-mask network to selectively force selected constant logic values into all scan cells in selected scan chains, and wherein said finite-state machine further comprises using a load signal to preset said input chain-mask controller with a predetermined state to selectively force said selected constant logic values into all said scan cells in said selected scan chains.

Claim 64 (CANCELLED).

65. (CURRENTLY AMENDED) ~~The input chain-mask controller of claim 62,~~ An input chain-mask controller for generating a plurality of input-mask enable signals for debug, diagnosis, and/or yield improvement of a scan-based integrated circuit in a selected scan-test mode or selected self-test mode, the scan-based integrated

circuit containing a plurality of scan chains, a plurality of pattern generators, a plurality of pattern compactors, and an input-mask network, each scan chain comprising multiple scan cells coupled in series; said input chain-mask controller comprising:

a finite-state machine for generating said input-mask enable signals for controlling said input-mask network to selectively force selected constant logic values into all scan cells in selected scan chains; and wherein said finite-state machine is selectively a shift register (SR) or a range decoder.

Claim 66 (CANCELLED).

Claims 67 - 89 (CANCELLED).